IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Coke S. Reed		
Assignee:	National Security Agency		
Title:	MULTIPLE LEVEL MINIMUM LOGIC NETWORK		
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Newport Beach, California
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BOX PATENT APPLICATION
Commissioner For Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

The following Amendment is submitted for entry into the above-referenced application filed on May 7, 2001.

AMENDMENTS

Please amend the above-referenced application as follows:

In the Specification

On page 1, kindly enter as the first line of the specification as follows:

This is a divisional of Application No. 09/397,333, filed September 14, 1999, which is a divisional of Application No. 08/505,513, filed July 21, 1995, now U.S. Patent No. 5,996,020.

Kindly replace the section beginning on page 4, line 21, ending on page 5, line 9, as follows:

In accordance with one aspect of the present invention, an interconnect apparatus includes a plurality of nodes and a plurality of interconnect lines selectively connecting the nodes in a multiple

level structure in which the levels include a richly interconnected collection of rings. The multiple level structure includes a plurality of J+1 levels in a hierarchy of levels and a plurality of $2^J K$ nodes at each level. If integer K is an odd number, the nodes on a level M are situated on 2^{J-M} rings with each ring including $2^M K$ nodes. Message data leaves the interconnect structure from nodes on a level zero. Each node has multiple communication terminals. Some are message data input and output terminals. Others are control input and output terminals. For example, a node A on level 0, the innermost level, receives message data from a node B on level 0 and also receives message data from a node C on level 1. Node A sends message data to a node D on level 0 and also sends message data to a device E that is typically outside the interconnect structure. One example of a device E is an input buffer of a computational unit. Node A receives a control input signal from a device F which is commonly outside the interconnect structure. An example of a device F is an input buffer of a computational unit. Node A sends a control signal to a node G on level 1.

In the Drawings

New drawings are being submitted concurrently with this amendment.

In the Claims

Please cancel all previous claims and file a divisional application including the following new claims:

39. (New) An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with each device in device set A being capable of sending data to a node in the node set T;

a device set Z mutually exclusive of the node set T with each device in device set Z being capable of receiving data from a node in the node set T;

a collection C of node sets that are subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C;

for a device x in the device set Z, a sequence cx = cx_0, cx_1, cx_2, … , cx_J exists with each member of the sequence cx being a node set in the collection C, the sequence cx being capable of passing data from devices in the device set A to the device x on a plurality of paths, among the plurality of paths being a path set P(x) characterized in that a path R is included in the path set P(x) only if each node on the path R is a member of the sequence cx, a node of the path R that receives a message directly from a device in device set A having the form cx_U and a node of the path R that sends data directly to the device x being of the form cx_V with U being larger than V;

for a member Q of the collection C, a corresponding set of devices Z(Q) exists in the device plurality Z such that a device q is included in the set of devices Z(Q) only if the member Q is also a member of the sequence cq;

for members cx_H and cx_K of the sequence cx with H > K, a device set Z(cx_K) is a subset of a device set Z(cx_H) and a device exists in device set Z(cx_H) that is not included in the device set Z(cx_K); and

the node set T includes three distinct nodes p, q, and r, the node p being in a member cz_D of sequence cz, the nodes q and r being in a member cz_E of the sequence cz with D > E, in one path of paths P(x) a message moves directly from the node p to the node r and in another path of paths P(x) a message moves directly from the node q to the node r.

40. (New) An interconnect structure according to Claim 39 wherein:

paths P(x) include a path such that if a message hops from a node in a member cz_n to a node in a member cz_m, then $n \geq m$.

41. (New) An interconnect structure according to Claim 39 wherein:

the collection C includes distinct member node sets D and E, and for corresponding device sets Z(D) and Z(E) with the device set Z(D) being a subset of the device set Z(E), a device y in the device set Z(D) exists such that member node set D is a node set cy_R and member node set E is a node set cy_S and R is greater than S.

42. (New) An interconnect structure according to Claim 39 further comprising:

an arrangement of the nodes in the interconnect structure into a hierarchy of levels of node sets L = L_0, L_1, …. L_J, each member of the hierarchy L being a node set that is subset

of the node set T and each node in the node set T is contained in exactly one member of the node sets L; and

for the device x of the device set Z, node set cx_N is a subset of the level N node set L_N, with N not exceeding J.

43. (New) An interconnect structure according to claim 42 wherein:

a message M_y targeted for a device y in the device set Z enters at a node on level L_J and exits at an output port on level L_0 with the output port being connected to the device y; and

for a hop in a path of the message M_y from a node of L_U to a node of L_V, U being greater than or equal to V.

44. (New) An interconnect structure according to claim 43 wherein:

the collection C includes 2^{J-N} members on a level N;

the collection C includes three members D, E and F such that member node set D is on the level L_N and member node sets E and F are on the level L_{N-1};

the interconnect set I includes interconnects positioned to allow data to pass directly from the member node set D to the member node set E and to pass directly from the node set D to the node set F; and

the device set Z includes device sets Z(D), Z(E), and Z(F) that correspond to the three members D, E, and F, the device sets Z(E) and Z(F) being mutually exclusive device sets, and device set Z(D) is the union of the device sets Z(E) and Z(F).

45. (New) An interconnect structure according to Claim 39 further comprising:

a member node set c in the collection C; and

a plurality of interconnects in the interconnect set I connecting nodes in the member c so that the nodes of the node set c are arranged in a ring.

46. (New) An interconnect structure in accordance with Claim 39 further comprising:

a logic L_p associated with the node p wherein for a message Mp that arrives at the node p, the logic Lp uses information concerning the sending of messages from node q for the logic Lp to determine where the node p is to send the message Mp.

47. (New) An interconnect structure according to claim 46 wherein:

the node q has priority over the node p to send data to the node r so that a message Mq located at the node q is not blocked from being sent to the node r by a message Mp at the node p.

48. (New) An interconnect structure according to claim 47 wherein;

the node q is capable of sending a control signal to the node p wherein the purpose of the control signal is to enforce the priority of the node q over the node p to send data to the node r.

49. (New) An interconnect structure according to Claim 39 wherein:

the node set T is a proper subset of nodes in the interconnect structure; and

the interconnect set I is a proper subset of the interconnects in the interconnect structure.

50. (New) An interconnect structure according to Claim 39 wherein:

each node in the interconnect structure is included in the node set T; and

each interconnect in the interconnect structure is included in the interconnect set I.

51. (New) An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with each device in device set A being capable of sending data to a node in the node set T;

a device set Z mutually exclusive of the node set T with each device in device set Z being capable of receiving data from a node in the node set T;

a collection C of node sets that are subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C;

for a device x in the device set Z, a sequence $cx = cx_0, cx_1, cx_2, \ldots, cx_J$ exists with each member of the sequence cx being a node set in the collection C, the sequence cx being capable of passing data from devices in the device set A to the device x on a

plurality of paths, among the plurality of paths being a path set P(x) characterized in that a path R is included in the path set P(x) only if each node on the path R is a member of the sequence cx, a node of the path R that receives a message directly from a device in device set A having the form cx_U and a node of the path R that sends data directly to the device x being of the form cx_V with U being larger than V;

for a member Q of the collection C, a corresponding set of devices Z(Q) exists in the device plurality Z such that a device q is included in the set of devices Z(Q) only if the member Q is also a member of the sequence cq;

for members cx_H and cx_K of the sequence cx with $H > K$, a device set $Z(cx_K)$ is a subset of a device set $Z(cx_H)$ and a device exists in device set $Z(cx_H)$ that is not included in the device set $Z(cx_K)$; and

the node set T includes three distinct nodes p, q, and r, the nodes p and q being in a member cz_D of sequence cz, the node r being in a member cz_E of the sequence cz with $D > E$, in a first path of paths P(x) a message moves directly from the node p to the node q, in a second path of paths P(x) a message moves directly from the node p to the node r, in a third path of paths P(x) a message moves from the node q to the node r.

52. (New) An interconnect structure according to Claim 51 wherein:

paths P(x) include a path such that if a message hops from a node in a member cz_n to a node in a member cz_m, then $n \geq m$.

53. (New) An interconnect structure according to Claim 51 further comprising:

an arrangement of the nodes in the interconnect structure into a hierarchy of levels of node sets $L = L_0, L_1, \ldots L_J$, each member of the hierarchy L being a node set that is subset of the node set T and each node in the node set T is contained in exactly one member of the node set L; and

for the device x of the device set Z, member node set cz_N is a subset of the level N node set L_N, N not exceeding J.

54. (New) An interconnect structure according to Claim 53 wherein:

a message M_y targeted for a device y in the device set Z enters at a node on level L_J and exits at an output port on level L_0 with the output port being connected to the device y; and

for a hop in a path of the message M_y from a node of L_U to a node of L_V, U being greater than or equal to V.

55. (New) An interconnect structure according to Claim 54 wherein:

the collection C includes 2^{J-N} members on a level N;

the collection C includes three members D, E and F such that member node set D is on the level L_N and member node sets E and F are on the level L_{N-1};

the interconnect set I includes interconnects positioned to allow data to pass directly from the member node set D to the member node set E and to pass directly from the node set D to the node set F; and

the device set Z includes device sets Z(D), Z(E), and Z(F) that correspond to the three members D, E, and F, the device sets Z(E) and Z(F) being mutually exclusive device sets, and device set Z(D) is the union of the device sets Z(E) and Z(F).

56. (New) An interconnect structure according to Claim 51 further comprising:

a member node set c in the collection C; and

a plurality of interconnects in the interconnect set I connecting nodes in the member c so that the nodes of the node set c are arranged in a ring.

57. (New) An interconnect structure comprising:

a plurality of nodes including a node N_E and a node set P, the node set P including a plurality of nodes that are capable of sending data to the node N_E; and

a plurality of interconnect paths interconnecting the plurality of nodes, the interconnect paths including data interconnect paths that couple nodes in pairs, a node pair including a sending node and a receiving node, the sending node being capable of sending data to the receiving node;

the nodes in the node set P having a priority relationship for sending data to the node N_E, the nodes in the node set P including distinct nodes N_F and N_A, the node N_F having a highest priority among the nodes in the node set P for sending data to the node N_E so that the message M_F arriving at the node N_F is not blocked from traveling to the node N_E by the message M_A arriving at the node N_A; and

for a message M arriving at the node N_A and the message M is blocked from being sent to the node N_E, then the blocking of message M from being sent to the node N_E causes sending of the message M from the node N_A to a node distinct from the node N_E.

58. (New) An interconnect structure according to Claim 57 wherein:
the node N_F is capable of sending data to a node N_T distinct from N_F and N_E.

59. (New) An interconnect structure according to Claim 57 wherein:
a node N_U of the node set P is not blocked from sending data to the node N_E as a result of data sent to the node N_E from a node N_V having a priority lower than the node N_U for sending data to the node N_E.

60. (New) An interconnect structure according to Claim 57 wherein:
the priority relationship among the nodes in the node set P capable of sending data to the node N_E depends on the position of the individual nodes in the node set P within the interconnect structure.

61. (New) An interconnect structure according to Claim 57 further comprising:
the plurality of nodes including the distinct nodes N_A, N_E, and N_F;
a plurality of logic elements associated with the plurality of nodes;
a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;
a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;
the plurality of nodes including:
a logic L_A associated with the node N_A that makes routing decisions for the node N_A;
a data interconnect path from the node N_F operative as the sending node to the node N_E operative as the receiving node;
a data interconnect path from the node N_A operative as the sending node to the node N_E operative as the receiving node; and

a control signal interconnect path from a source associated with the node N_F operative as a sending node to the logic L_A, the control signal enforcing a priority for sending data from the node N_F to the node N_E over sending data from the node N_A to the node N_E.

62. (New) An interconnect structure according to Claim 57 further comprising:

the plurality of nodes including the node N_F, the node N_A, and a node set R, the nodes N_F and N_A being distinct nodes that are excluded from the node set R, the node N_A being capable of sending data to each node in the node set R;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to the logic L_A associated with the node N_A, the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set R the node N_A sends data.

63. (New) An interconnect structure according to Claim 57 wherein:

the plurality of nodes include the nodes N_A, N_D, N_E, and N_F;

the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of interconnect paths further include data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect path for sending a control signal from a source associated with the node N_F to the logic element L_A associated with node N_A, and

for a message M arriving at the node N_F, a source associated with the node N_F sends a control signal S to the logic element L_A, the logic element L_A using the control signal S to determine between sending the message M to the node N_E or to the node N_D.

64. (New) An interconnect structure according to Claim 57 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including distinct nodes N_F, N_A, N_E, and N_D;

the plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

the plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a message M passing through the node N_A, a control signal S received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

65. (New) An interconnect structure according to Claim 57 further comprising:

one or more output ports in which each output port that is accessible from the node N_F is also accessible from the node N_E.

66. (New) An interconnect structure according to Claim 57 further comprising:

one or more output ports in which an output port that is accessible from the node N_A is not accessible from the node N_E.

67. (New) An interconnect structure according to Claim 57 further comprising:

distinct nodes N_A and N_F of the plurality of nodes;

means for sending a plurality of messages including a message M_A and a message M_F through the interconnect structure nodes, the message M_F including one or more header bits;

means for routing the message M_F to enter the node N_F of the interconnect structure;

means for routing the message M_A to enter the node N_A of the interconnect structure; and

means for using header bits of the message M_F at the node N_F to route the message M_A from the node N_A.

68. (New) An interconnect structure comprising:

a plurality of nodes including a node N_E and a node set P, the node set P including a plurality of nodes that are capable of sending data to the node N_E; and

a plurality of interconnect paths interconnecting the plurality of nodes, the interconnect paths including data interconnect paths that couple nodes in pairs including a receiving node and a sending node that is capable of sending data to the receiving node; and

the nodes in the node set P having a priority relationship for sending data to the node N_E, the nodes in the node set P including distinct nodes N_F and N_A, the node N_F having a highest priority among the nodes in the node set P for sending data to the node N_E, the message M_F arriving at the node N_F is not blocked from traveling to the node N_E by the message M_A arriving at the node N_A, wherein:

when a message M arrives at the node N_A and is targeted for the node N_E and not blocked by a message M' arriving at a node in the node set P having a higher priority than the node N_A for sending messages to the node N_E, the node N_A sends the message M to the node N_E.

69. (New) An interconnect structure according to Claim 68 wherein:

the node N_F is capable of sending data to a node N_T distinct from N_F and N_E.

70. (New) An interconnect structure according to Claim 68 wherein:

a node N_U of the node set P is not blocked from sending data to the node N_E as a result of data sent to the node N_E from a node N_V having a priority lower than the node N_U for sending data to the node N_E.

71. (New) An interconnect structure according to Claim 68 wherein:

the priority relationship among the nodes in the node set P capable of sending data to the node N_E depends on the position of the individual nodes in the node set P within the interconnect structure.

72. (New) An interconnect structure according to Claim 68 further comprising:

the plurality of nodes including the distinct nodes N_A, N_E, and N_F;

a plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

a logic L_A associated with the node N_A that makes routing decisions for the node N_A;

a data interconnect path from the node N_F operative as the sending node to the node N_E operative as the receiving node;

a data interconnect path from the node N_A operative as the sending node to the node N_E operative as the receiving node; and

a control signal interconnect path from a source associated with the node N_F operative as a sending node to the logic L_A, the control signal enforcing a priority for sending data from the node N_F to the node N_E over sending data from the node N_A to the node N_E.

73. (New) An interconnect structure according to Claim 68 further comprising:

the plurality of nodes including the node N_F, the node N_A, and a node set R, the nodes N_F and N_A being distinct nodes that are excluded from the node set R, the node N_A being capable of sending data to each node in the node set R;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to the logic L_A associated with the node N_A, the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set P the node N_A sends data.

74. (New) An interconnect structure according to Claim 68 wherein:

the plurality of nodes include the nodes N_A, N_D, N_E, and N_F;

the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of interconnect paths further include data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect path for sending a control signal from a source associated with the node N_F to the logic element L_A associated with node N_A, and

for a message M arriving at the node N_F, a source associated with the node N_F sends a control signal S to the logic element L_A, the logic element L_A using the control signal S to determine between sending the message M to the node N_E or to the node N_D.

75. (New) An interconnect structure according to Claim 68 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including distinct nodes N_F, N_A, N_E, and N_D;

the plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

the plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a message M passing through the node N_A, a control signal S received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

76. (New) An interconnect structure according to Claim 68 further comprising:

one or more output ports in which each output port that is accessible from the node N_F is also accessible from the node N_E.

77. (New) An interconnect structure according to Claim 68 further comprising:

one or more output ports in which an output port that is accessible from the node N_A is not accessible from the node N_E.

78. (New) An interconnect structure according to Claim 68 further comprising:

distinct nodes N_A and N_F of the plurality of nodes;

means for sending a plurality of messages including a message M_A and a message M_F through the interconnect structure nodes, the message M_F including one or more header bits;

means for routing the message M_F to enter the node N_F of the interconnect structure;

means for routing the message M_A to enter the node N_A of the interconnect structure; and

means for using header bits of the message M_F at the node N_F to route the message M_A from the node N_A.

79. (New) An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive with the node set T with each device in device set A capable of sending data to a node in node set T;

a device set Z mutually exclusive with the node set T with each device in device set Z capable of receiving data from a node in node set T;

a set of data-carrying paths P, each path of path set P being capable of carrying data from a device in the device set A to a device in the device set Z, each node on the path of path set P is included in the node set T, and each interconnect in the path is included in the interconnect set I;

a node set U characterized as the set of nodes within the node set T that are on a path included in the path set P;

for a node N in the node set T such that the node N is on a path in the path set P, a corresponding set of devices Z(N) exists in the device set Z such that a device w is included in the device set Z(N) only if a path exists in the path set P from a member of the device set A to the device w such that the path contains the node N; and

the node set U includes three distinct nodes N_A, N_D, and N_E such that node N_A is capable of sending data to node N_D and node N_E, and device set $Z(N_A)$ is the same as device set $Z(N_D)$, and device set $Z(N_E)$ is a proper subset of device set $Z(N_A)$.

80. (New) An interconnect structure according to Claim 79 wherein:

the interconnect S is a part of a larger interconnect structure T.

81. (New) An interconnect structure according to Claim 79 further comprising:

the interconnect S is not a subset of a larger interconnect structure T.

82. (New) An interconnect structure according to Claim 79 wherein:

a time T_A is associated with the node N_A such that messages arriving at the node N_A are sent to another node within the time T_A of the messages' arrival at the node N_A.

83. (New) An interconnect structure according to Claim 79 further comprising:

a logic element L_A associated with the node N_A that determines routing from the node N_A;

a node N_X distinct from the node N_A;

a logical element L_X associated with the node N_X that determines routing for the node N_X, the logical element L_X being distinct from the logical element L_A.

84. (New) An interconnect structure according to Claim 79 further comprising:

the plurality of nodes including a node N_F, the nodes N_A, N_E, and N_F being mutually distinct;

a plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

the plurality of nodes including:

a logic L_A associated with the node N_A that makes routing decisions for the node N_A;

a data interconnect path from the node N_F operative as the sending node to the node N_E operative as the receiving node;

a data interconnect path from the node N_A operative as the sending node to the node N_E operative as the receiving node; and

a control signal interconnect path from a source associated with the node N_F operative as a sending node to the logic L_A, the control signal enforcing a priority for sending data from the node N_F to the node N_E over sending data from the node N_A to the node N_E.

85. (New) An interconnect structure according to Claim 79 further comprising:

the plurality of nodes including a node N_F and a node set R, the nodes N_F and N_A being distinct nodes that are excluded from the node set R, the node N_A being capable of sending data to each node in the node set R;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to the logic L_A associated with the node N_A, the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set R the node N_A sends data.

86. (New) An interconnect structure according to Claim 85 wherein:
the node N_A is capable of sending data only to nodes in the node set R.

87. (New) An interconnect structure according to Claim 85 wherein:
the node N_A is capable of sending data to a node outside the node set R.

88. (New) An interconnect structure according to Claim 79 wherein:
the plurality of nodes include a node N_F;
the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;
the plurality of interconnect paths further include data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect path for sending a control signal from a source associated with the node N_F to the logic element L_A associated with node N_A, and
for a message M arriving at the node N_F, a source associated with the node N_F sends a control signal S to the logic element L_A, the logic element L_A using the control signal S to determine between sending the message M to the node N_E or to the node N_D.

89. (New) An interconnect structure according to Claim 88 wherein:
a message M' arriving at the node N_A is routed to a node N_Z distinct from the nodes N_E, N_D, and N_F.

90. (New) An interconnect structure according to Claim 88 wherein:

the control interconnect path from the node N_F to the node N_A is a direct link from a logic L_F associated with the node N_F to the logic L_A.

91. (New) An interconnect structure according to Claim 88 wherein:

the control signal sent to the node N_A is tapped from an output data port of the node N_F.

92. (New) An interconnect structure according to Claim 79 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including a node N_F, the nodes N_F, N_A, N_E, and N_D being mutually distinct;

the plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

the plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a message M passing through the node N_A, a control signal S received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

93. (New) An interconnect structure according to Claim 92 wherein:

the control signal interconnection path is a direct link from the node N_F to the node N_A.

94. (New) An interconnect structure according to Claim 92 wherein:

routing of a message M' passing through the node N_A is the same whether the control signal from the node N_F is the control signal S or the control signal S'.

95. (New) An interconnect structure according to Claim 92 wherein:
the control signal sent to the logic L_A is tapped from an output data port of the node N_F.

96. (New) An interconnect structure according to Claim 79 further comprising:
distinct nodes N_A and N_F of the plurality of nodes;
means for sending a plurality of messages including a message M_A and a message M_F through the interconnect structure nodes, the message M_F including one or more header bits;
means for routing the message M_F to enter the node N_F of the interconnect structure;
means for routing the message M_A to enter the node N_A of the interconnect structure; and
means for using header bits of the message M_F at the node N_F to route the message M_A from the node N_A.

97. (New) An interconnect structure according to Claim 96 wherein:
the means for routing the message M_F uses the one or more header bits of the message M_F to route the message M_F; and
the means for routing the message M_A uses information relating to the routing of the message M_F to route the message M_A.

98. (New) An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:
a node set T;
an interconnect set I that selectively connects nodes in the node set T;
a device set A mutually exclusive with the node set T with each device in device set A capable of sending data to a node in node set T;
a device set Z mutually exclusive with the node set T with each device in device set Z capable of receiving data from a node in node set T;
a set of data-carrying paths P, each path being capable of carrying data from a device in the device set A to a device in the device set Z, each node on the path is included in the node set T, and each interconnect in the path is included in the interconnect set I;
a node set U characterized as the set of nodes within the node set T that are on a path included in the path set P;

for an interconnect link L in interconnect set I, the interconnect link L being an interconnect link on a path in the path set P, a corresponding set of devices Z(L) exists in the device set Z such that a device w is included in the device set Z(L) only if a path containing the interconnect link L in the path set P exists from a device in the device set A to the device w; and

the node set U includes distinct nodes N_A, N_D, and N_E such that node N_A is capable of sending data to the node N_D on a link L_{AD}, the node N_A is capable of sending data to the node N_E on a link L_{AE}, and the device set $Z(L_{AE})$ is a proper subset of the device subset $Z(L_{AD})$.

99. (New) An interconnect structure according to Claim 98 wherein:

the interconnect S is a part of a larger interconnect structure T.

100. (New) An interconnect structure according to Claim 98 further comprising:

the interconnect S is not a subset of a larger interconnect structure T.

101. An interconnect structure according to Claim 98 wherein:

a time T_A is associated with the node N_A such that messages arriving at the node N_A are sent to another node within the time T_A of the messages' arrival at the node N_A.

102. (New) An interconnect structure according to Claim 98 further comprising:

a logic element L_A associated with the node N_A that determines routing from the node N_A;

a node N_X distinct from the node N_A;

a logical element L_X associated with the node N_X that determines routing for the node N_X, the logical element L_X being distinct from the logical element L_A.

103. (New) An interconnect structure according to Claim 98 further comprising:

the plurality of nodes including a node N_F, the nodes N_A, N_E, and N_F being mutually distinct;

a plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

the plurality of nodes including:

a logic L_A associated with the node N_A that makes routing decisions for the node N_A;

a data interconnect path from the node N_F operative as the sending node to the node N_E operative as the receiving node;

a data interconnect path from the node N_A operative as the sending node to the node N_E operative as the receiving node; and

a control signal interconnect path from a source associated with the node N_F operative as a sending node to the logic L_A, the control signal enforcing a priority for sending data from the node N_F to the node N_E over sending data from the node N_A to the node N_E.

104. (New) An interconnect structure according to Claim 98 further comprising:

the plurality of nodes including a node N_F and a node set R, the nodes N_F and N_A being distinct nodes that are excluded from the node set R, the node N_A being capable of sending data to each node in the node set R;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node N_F to the logic L_A associated with the node N_A, the logic L_A using a control signal from a source associated with the node N_F to determine to which node of the node set R the node N_A sends data.

105. (New) An interconnect structure according to Claim 104 wherein:

the node N_A is capable of sending data only to nodes in the node set R.

106. (New) An interconnect structure according to Claim 104 wherein:
the node N_A is capable of sending data to a node outside the node set R.

107. (New) An interconnect structure according to Claim 98 wherein:
the plurality of nodes include a node N_F;
the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;
the plurality of interconnect paths further include data interconnect paths for sending data from the node N_A to the node N_E and to the node N_D, and a control interconnect path for sending a control signal from a source associated with the node N_F to the logic element L_A associated with node N_A, and
for a message M arriving at the node N_F, a source associated with the node N_F sends a control signal S to the logic element L_A, the logic element L_A using the control signal S to determine between sending the message M to the node N_E or to the node N_D.

108. (New) An interconnect structure according to Claim 107 wherein:
a message M' arriving at the node N_A is routed to a node N_Z distinct from the nodes N_E, N_D, and N_F.

109. (New) An interconnect structure according to Claim 107 wherein:
the control interconnect path from the node N_F to the node N_A is a direct link from a logic L_F associated with the node N_F to the logic L_A.

110. (New) An interconnect structure according to Claim 107 wherein:
the control signal sent to the node N_A is tapped from an output data port of the node N_F.

111. (New) An interconnect structure according to Claim 98 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including a node N_F, the nodes N_F, N_A, N_E, and N_D being mutually distinct;

the plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

the plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element L_A associated with the node N_A, the logical element L_A that uses a control signal from a source associated with the node N_F to determine where to route a message M passing through the node N_A, a control signal S received from a source associated with the node N_F that causes sending of the message M from the node N_A to the node N_E, and a control signal S' received from the node N_F that causes sending of the message M from the node N_A to the node N_D.

112. (New) An interconnect structure according to Claim 111 wherein:

the control signal interconnection path is a direct link from the node N_F to the node N_A.

113. (New) An interconnect structure according to Claim 111 wherein:

routing of a message M' passing through the node N_A is the same whether the control signal from the node N_F is the control signal S or the control signal S'.

114. (New) An interconnect structure according to Claim 111 wherein:

the control signal sent to the logic L_A is tapped from an output data port of the node N_F.

115. (New) An interconnect structure according to Claim 98 further comprising:

distinct nodes N_A and N_F of the plurality of nodes;

means for sending a plurality of messages including a message M_A and a message M_F through the interconnect structure nodes, the message M_F including one or more header bits;

means for routing the message M_F to enter the node N_F of the interconnect structure;

means for routing the message M_A to enter the node N_A of the interconnect structure; and

means for using header bits of the message M_F at the node N_F to route the message M_A from the node N_A.30.

116. (New) An interconnect structure according to Claim 115 wherein:

the means for routing the message M_F uses the one or more header bits of the message M_F to route the message M_F; and

the means for routing the message M_A uses information relating to the routing of the message M_F to route the message M_A.

CONCLUSION

The application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

EXPRESS MAIL LABEL NO:
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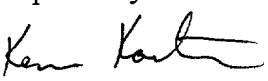
Respectfully submitted,



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ATTACHMENT A

This amendment adds the following as the first line of the specification:

--This is a divisional of Application No. 09/397,333, filed September 14, 1999, which is a divisional of Application No. 08/505,513, filed July 21, 1995, now U.S. Patent No. 5,996,020.--

The amendments to the paragraph beginning on page 4, line 21, ending on page 5, line 9, are as follows:

In accordance with one aspect of the present invention, an interconnect apparatus includes a plurality of nodes and a plurality of interconnect lines selectively connecting the nodes in a multiple level structure in which the levels include a richly interconnected collection of rings. The multiple level structure includes a plurality of J+1 levels in a hierarchy of levels and a plurality of $2^{J}K$ nodes at each level. If integer K is an odd number, the nodes on a level M are situated on 2^{J-M} rings with each ring including $2^{M}K$ nodes. Message data leaves the interconnect structure from nodes on a level zero. Each node has multiple communication terminals. Some are message data input and output terminals. Others are control input and output terminals. For example, a node A on level 0, the innermost level, receives message data from a node B on level 0 and also receives message data from a node C on level 1. Node A sends message data to a node D on level 0 and also sends message data to a device E that is typically outside the interconnect structure. One example of a device E is an input buffer of a computational unit. Node A receives a control input signal from a device F which is commonly outside the interconnect structure. An example of a device F is an [output] input buffer of a computational unit. Node A sends a control signal to a node G on level 1.